Amendments to the Claims:

The following listing of claims replaces all prior versions of the claims:

Listing of Claims:

1. (original) A method comprising:

creating a filter structure using a parameter of a periodic pulse train, the filter structure having a plurality of time slots, each time slot being associated with a memory value;

receiving a pulse at a time;

incrementing the memory value associated with the time slot corresponding to the time the pulse was received;

filtering the pulse if the memory value exceeds a threshold; and

transmitting the pulse to a processor if the memory value does not exceed the threshold.

2. (original) The method of claim 1, where the parameter is a time slot width.

3. (original) The method of claim 1, where the parameter is a number of time slots.

4. (currently amended) The method of claim 1, where the filter structure includes a length, and the creating includes using (a) a time slot width and (b) a number of time slots to match the length of the filter structure with a pulse repetition interval of the periodic pulse train.

5. (original) The method of claim 1, where the parameter is a modification parameter.

6. (original) The method of claim 5, where the modification parameter is the width of a last time slot of the filter structure.

7. (original) The method of claim 1, where the parameter is the threshold.

8. (original) The method of claim 1, where the filtering includes deleting the pulse.

9. (currently amended) A data storage device ~~computer readable medium~~ comprising machine readable instructions for:

creating a filter structure using a parameter of a periodic pulse train, the filter structure having a plurality of time slots, each time slot being associated with a memory value;

receiving a pulse at a time;

incrementing the memory value associated with the time slot corresponding to the time the pulse was received;

filtering the pulse if the memory value exceeds a threshold; and

transmitting the pulse to a processor if the memory value does not exceed the threshold.

10. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the parameter is a time slot width.

11. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the parameter is a number of time slots.

12. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the filter structure includes a length, and the creating includes using (a) a time slot width and (b) a number of time slots to match the length of the filter structure with a pulse repetition interval of the periodic pulse train.

13. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the parameter is a modification parameter.

14. (currently amended) The data storage device ~~computer readable medium~~ of claim 13, where the modification parameter is the width of a last time slot of the filter structure.

15. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the parameter is the threshold.

16. (currently amended) The data storage device ~~computer readable medium~~ of claim 9, where the filtering includes deleting the pulse.

17. (currently amended) An apparatus comprising:

an input filter;

a pulse detection circuit coupled to the input filter;

a periodic pulse filter coupled to the pulse detection circuit, the periodic pulse filter~~ing circuit~~ operable to:

use a parameter to create a filter structure, the filter structure having a plurality of time slots, each time slot being associated with a memory value;

receive a pulse at a time;

increment the memory value associated with the time slot corresponding to the time the received pulse arrived, and

filter the pulse if the memory value exceeds a threshold; and

a pulse queuing and transmission circuit coupled to the periodic pulse filter.

18. (original) The apparatus of claim 17, further comprising an analog-to-digital converter coupled to the input filter.

19. (original) The apparatus of claim 17, further comprising a processor coupled to the pulse queuing and transmission circuit.